CLAIMS

What is claimed is:

1. A method of providing CPU functional testing, the method comprising:
executing operations on multiple functional units of a same type in the CPU;
automatically comparing outputs from the multiple functional units; and
checking results of the comparison only for redundant operations.

2. The method of claim 1, wherein automatically comparing the outputs from the multiple functional units is performed by comparator circuitry within the CPU that is coupled to receive the outputs.

3. The method of claim 2, further comprising:
setting a comparison flag based on output of the comparator circuitry.

4. The method of claim 3, wherein checking results of the comparison is performed by examining the comparison flag.

5. The method of claim 4, further comprising:
if examination of the comparison flag indicates an error, then halting the execution and providing a notification of the error.

6. The method of claim 1, wherein the redundant operations are opportunistically scheduled by a compiler to take advantage of an otherwise idle functional unit during a cycle.

7. The method of claim 6, wherein the compiler is configured with various levels of aggressiveness with respect to scheduling of the redundant operations.

8. The method of claim 7, wherein the levels of aggressiveness include levels more aggressive than just taking advantage of otherwise idle functional units.

9. The method of claim 8, wherein a high level of aggressiveness forces all operations on a functional unit to be performed redundantly on another functional unit of the same type.

10. The method of claim 1, wherein the functional units comprise floating point units.

11. The method of claim 1, wherein the functional units comprise arithmetic logic units.

12. A microprocessor with built-in functional testing capability, the microprocessor comprising:
multiple functional units of a same type;
registers that receive outputs from the multiple functional units; and
comparator circuitry that also receives the outputs from the multiple functional units and compares the outputs to provide functional testing.

13. The microprocessor of claim 12, wherein the multiple functional units comprise floating point units.

14. The microprocessor of claim 12, wherein the multiple functional units comprise arithmetic logic units.

15. The microprocessor of claim 12, wherein the microprocessor executes a program which is compiled by a compiler that opportunistically schedules redundant operations to take advantage of an otherwise idle functional unit during a cycle.

16. The microprocessor of claim 12, further comprising:
at least one flag coupled to receive results from the comparator circuitry.

17. The microprocessor of claim 16, wherein the flag is ignored if different operations are performed on the multiple functional units and is checked if a same redundant operation is performed on the multiple functional units.

18. A computer-readable program product for execution on a target microprocessor with multiple functional units of a same type, the program product comprising executable code that includes a redundant operation scheduled on two functional units to take advantage of one of the functional units that would otherwise be idle during a cycle.

19. The program product of claim 18, wherein the program product is configured to execute on a microprocessor having comparator circuitry to automatically compare outputs of the two functional units.

20. A apparatus for providing CPU functional testing, the apparatus comprising:
means for executing operations on multiple functional units of a same type in the CPU;
means for automatically comparing outputs from the multiple functional units; and
means for checking results of the comparison only for redundant operations.